REMARKS

Claims 9-15 and 21-23 are pending in the application.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 9 and 12 stand rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 6,114,051 to Nishimura et al.(hereinafter, Nishimura) in view of U.S. Patent No. 6,342,734 B1 to Allman et al. (hereinafter, Allman) and U.S. Patent No. 6,165,880) to Yuang et al. (hereinafter, Yuang). Claims 10, 13, and 14 stand rejected under 35 U.S.C. §103(a) as unpatentable over Nishimura in view of Allman and Yuang, and further in view of U.S. Patent Application No. 2003/0008467 A1 to Kai et al. (hereinafter, Kai). Claim 11 stands rejected under 35 U.S.C. §103(a) as unpatentable over Nishimura in view of Allman and Yuang, and further in view of U.S. Patent No. 5,891,799 to Tsui. Claim 15 stands rejected under 35 U.S.C. §103(a) as unpatentable over Nishimura in view of Allman and Yuang, and further in view of U.S. Patent No. 6,391,713 B1 to Hsue et al. (hereinafter, Hsue). Claim 22 stands rejected under 35 U.S.C. §103(a) as unpatentable over Nishimura in view of Allman and Yuang, and further in view of U.S. Patent No. 6,596,641 to Jost et al. (hereinafter, Jost).

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention, as defined in independent claim 9 (and similarly defined in claim 23), is directed to a method of fabricating a multilayer semiconductor device that comprises forming a metal-insulator-metal (MIM) capacitor including a first metal plate, a dielectric layer formed on the first metal plate, and a second metal plate formed on the dielectric layer, patterning the second metal plate, depositing a nitride etch stop layer above the MIM capacitor, forming an

interlayer dielectric on the nitride etch stop layer, forming a first via and a second via through at least the interlayer dielectric by an anisotropic etch process to contact the nitride etch stop layer above the patterned second metal plate and above the first metal plate, respectively, and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer.

An aspect of the present invention prevents degradation of the capacitor dielectric, which may be caused by excessive electrical charging and ion/plasma damage of the top and bottom plates of a metal-insulator-metal (MIM) capacitor during anisotropic etching, by depositing a nitride etch stop layer above at least the top metal plate and the bottom plate of the MIM capacitor.

Another aspect of the present invention prevents plate-to-plate electrical shorting of an MIM capacitor, which may be caused by either top plate etch-through or dielectric breakdown, associated with anisotropic etch processes above the level of the MIM capacitor, by depositing a nitride etch stop layer above at least the top metal plate and the bottom plate of the MIM capacitor.

II. THE PRIOR ART REJECTIONS

A. The Nishimura Reference

With respect to claims 9 and 23, the Examiner admits that Nishimura fails "to teach using the nitride layer as an etch stop layer; forming the first and second vias by an anisotropic etch process to contact the nitride layer; and removing portions of the nitride etch stop layer." (Please see, Office Action, page 3, lines 14-16).

B. The Allman Reference

Allman discloses that an optional dielectric layer 47 may be deposited on top of the top plate 44 to provide an etch stop for the via etched in the process of forming the via interconnect 46 extending from the upper interconnect layer 24 to the top plate 44 of the capacitor 20 (col. 6, lines 41-45). The dielectric layer 47 will thereby prevent a portion of the top plate 44 from being

etched away or degraded while the adjoining via continues to be etched through the IMD layer 26 to the top of the bottom plate 33 (col. 6, lines 48-52, and particularly, Figs. 1 and 4-6).

Claim 9 (and similarly claim 23) recites at least the features of "forming a first via and a second via through at least the interlayer dielectric by an anisotropic etch process to contact the nitride etch stop layer above the patterned second metal plate and above the first metal plate, respectively; and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer."

Applicants submit that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions. Specifically, Nishimura is directed to a semiconductor device having a MIM capacitor capable of being formed with less contamination in the active element region and having an excellent leakage current characteristic, whereas Allman is merely directed to preventing the growth of material grains in the interconnect layer which becomes one of the capacitor plates to avoid deformation of the capacitor plates. No person of ordinary skill in the art would refer to a patent for preventing material grain growth when attempting to reduce the contamination in the active region of a MIM capacitor. Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Therefore, Applicants submit that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Figs. 1 and 4-6 of Allman clearly show that the optional dielectric layer 47, which allegedly corresponds to the claimed invention's nitride etch stop layer, provides an etch stop for the via extending to the top plate of the capacitor, does not extend over the bottom plate 33, which allegedly corresponds to the claimed invention's first metal plate, of the capacitor 20, and thus, does not provide an etch stop for the via extending to the top of the bottom plate 33.

Therefore, Allman fails to teach or suggest at least the features of "forming a first via and a second via through at least the interlayer dielectric by an anisotropic etch process to contact the

nitride etch stop layer above the patterned second metal plate and above the first metal plate, respectively; and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer," as recited in claim 9 (and similarly in claim 23).

It is the Examiner's contention, however, that the silicon nitride layer 516 of Nishimura extends over the MIM capacitor.

Applicants, as discussed above, submit that these references would not have been combined as suggested by the Examiner. Specifically, the disclosure of Nishimura teaches away from the Examiner's suggested combination. Nishimura teaches forming through holes 519, 520 by a RIE process through the SiO_2 film 517 and the SiN_x film 516 to expose the top electrode 515 and the bottom electrode 513. A gold interconnect layer 525 is then formed in each of the holes in contact with the electrodes (see Nishimura Figures 5A through 5E).

The claimed invention teaches forming a first and second via by an anisotropic etch process (e.g., RIE) to contact a nitride etch stop layer. The nitride etch stop layer prevents the vias from contacting the top and bottom electrodes. There is no motivation or suggestion to combine an etch stop layer with the invention of Nishimura because Nishimura requires that the contact holes contact the top and bottom electrodes so that the gold interconnect layers may contact the electrodes. The etch stop layer would prevent the contact holes from contacting the electrode layers.

Therefore, Applicants submit that these references would not have been combined as suggested by the Examiner and that Allman and Nishimura (and any combination thereof) fail to teach or suggest at least the features of "forming a first via and a second via through at least the interlayer dielectric by an anisotropic etch process to contact the nitride etch stop layer above the patterned second metal plate and above the first metal plate, respectively; and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer," as recited in claim 9 (and similarly in claim 23).

C. The Yuang Reference

The Examiner admits that Nishimura and Allman fail to teach forming the first and

second vias through at least the interlayer dielectric by an anisotropic etch process to contact the nitride etch stop layer (Office Action, page 4, lines 10-12). The Examiner then continues to state, "However, Yuang et al. (Figs. 1-3) in a related method to form interconnects using a nitride etch stop layer teach[es] forming a first (1) and second (1') via through an interlayer dielectric (22) by an anisotropic etch process to contact a nitride etch stop layer (20) (column 5, lines 16-53)." (Office Action, page 4, lines 12-15).

Yuang does not cure the deficiencies of Nishimura and Allman, as argued above with respect to the rejection of claims 9 and 23. Nowhere does Yuang teach or suggest forming first and a second vias through an interlayer dielectric by an anisotropic etch process to contact a nitride etch stop layer, which is disposed above a patterned second metal plate and above a first metal plate, respectively, of an MIM capacitor and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer as recited in claim 9.

For at least the reasons outlined above, Applicants respectfully submit that Nishimura, Allman and Yuang, either individually or in combination, fail to disclose every feature of claims 9 and 23. Accordingly, Nishimura, Allman and Yuang, either individually or in combination, fail to teach or suggest the subject matter of claims 9 and 23, as well as claims 12 and 21, which depend from claim 9, under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 9, 12, 21 and 23 under 35 U.S.C. §103(a) as unpatentable over Nishimura in view of Allman and Yuang is respectfully solicited.

D. The Kai Reference

With respect to claims 10, 13 and 14, the Examiner cites Figs. 5-11 of Kai for teaching patterning of a second metal plate (36) using an anisotropic etching process ([0045-0050]) (Office Action, page 5, lines 13-15).

Kai does not cure the deficiencies of Nishimura, Allman and Yuang, as argued above with respect to the rejection of claims 9, 12, 21 and 23 because nowhere does Kai teach or suggest forming first and a second vias through an interlayer dielectric by an anisotropic etch

process to contact a nitride etch stop layer, which is disposed above a patterned second metal plate and above a first metal plate, respectively, of an MIM capacitor and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer as recited in claim 9.

For at least the reasons outlined above, Applicants respectfully submit that Nishimura, Allman, Yuang and Kai, either individually or in combination, fail to disclose every feature of claim 9. Accordingly, Nishimura, Allman, Yuang and Kai, either individually or in combination, fail to teach or suggest the subject matter of claim 9 and claims 10, 13 and 14, which depend from claim 9, under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 10, 13 and 14 under 35 U.S.C. §103(a) as unpatentable over Nishimura, in view of Allman and Yuang, as applied to claims 9, 12, 21 and 23, and further in view of Kai is respectfully solicited.

E. The Tsui Reference

With respect to claim 11, the Examiner cites Fig. 6 of Tsui for teaching removing portions of a nitride layer (16) using C_4H_8 (column 5, lines 20-65).

Tsui does not cure the deficiencies of Nishimura, Allman and Yuang, as argued above with respect to the rejection of claims 9, 12, 21 and 23 because nowhere does Tsui teach or suggest forming first and a second vias through an interlayer dielectric by an anisotropic etch process to contact a nitride etch stop layer, which is disposed above a patterned second metal plate and above a first metal plate, respectively, of an MIM capacitor and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer as recited in claim 9.

For at least the reasons outlined above, Applicants respectfully submit that Nishimura, Allman, Yuang and Tsui, either individually or in combination, fail to disclose every feature of claim 9. Accordingly, Nishimura, Allman, Yuang and Tsui, either individually or in combination, fail to teach or suggest the subject matter of claim 9 and claim 11, which depends from claim 9, under 35 U.S.C. §103(a). Withdrawal of the rejection of claim 11 under 35 U.S.C. §103(a) as unpatentable over Nishimura, in view of Allman and Yuang, as applied to claims 9,

12, 21 and 23 and further in view of Tsui is respectfully solicited.

F. The Hsue Reference

With respect to claim 15, the Examiner cites Hsue for forming a second interlayer dielectric between the second metal plate and the nitride etch stop layer (Office Action, page 7, lines 7-8).

Hsue does not cure the deficiencies of Nishimura, Allman and Yuang, as argued above with respect to the rejection of claims 9, 12, 21 and 23 because nowhere does Hsue teach or suggest forming first and a second vias through an interlayer dielectric by an anisotropic etch process to contact a nitride etch stop layer, which is disposed above a patterned second metal plate and above a first metal plate, respectively, of an MIM capacitor and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer as recited in claim 9.

For at least the reasons outlined above, Applicants respectfully submit that Nishimura, Allman, Yuang and Hsue, either individually or in combination, fail to disclose every feature of claim 9. Accordingly, Nishimura, Allman, Yuang and Hsue, either individually or in combination, fail to teach or suggest the subject matter of claim 9 and claim 15, which depends from claim 9, under 35 U.S.C. §103(a). Withdrawal of the rejection of claim 15 under 35 U.S.C. §103(a) as unpatentable over Nishimura, in view of Allman and Yuang, as applied to claims 9, 12, 21 and 23, and further in view of Hsue is respectfully solicited.

G. The Jost Reference

With respect to claim 22, the Examiner cites Figures 1-6 of Jost for teaching a method to form a contact hole by forming a silicon nitride layer on a surface of a substrate, etching the silicon oxide layer using a dry etching process and etching the silicon nitride layer using either a dry or wet etching process (see Office Action, page 8, lines 11-17).

Jost does not, however, cure the deficiencies of Nishimura, Allman and Yuang, as argued above with respect to the rejection of claims 9, 12, 21 and 23 because nowhere does Jost teach or

suggest forming first and a second vias through an interlayer dielectric by an anisotropic etch process to contact a nitride etch stop layer, which is disposed above a patterned second metal plate and above a first metal plate, respectively, of an MIM capacitor and removing portions of the nitride etch stop layer, where the first via and the second via contact the nitride etch stop layer as recited in claim 9.

For at least the reasons outlined above, Applicants respectfully submit that Nishimura, Allman, Yuang and Jost, either individually or in combination, fail to disclose every feature of claim 9. Accordingly, Nishimura, Allman, Yuang and Jost, either individually or in combination, fail to teach or suggest the subject matter of claim 9 and claim 22, which depends from claim 9, under 35 U.S.C. §103(a). Withdrawal of the rejection of claim 22 under 35 U.S.C. §103(a) as unpatentable over Nishimura, in view of Allman and Yuang, as applied to claims 9, 12, 21 and 23, and further in view of Jost is respectfully solicited.

III. INFORMAL MATTERS AND CONCLUSION

In response to the Examiner's objection of the Information Disclosure Statement filed on January 16, 2003, Applicants records do not indicate that an Information Disclosure Statement was filed on that date. Applicants submit that an IDS was filed with the Application on November 25, 2002. Applicants have reviewed the IDS filed on November 25, 2002 and it does not appear to include a citation number P03. Applicants respectfully request the Examiner to confirm his objection.

In view of the foregoing, Applicants submit that claims 9-15 and 21-23, all of the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Amendment by facsimile with the United States Patent and Trademark Office to Examiner Julio J. Maldonado, Group Art Unit 2823 at fax number (703) 872-9306 this 13th day of September, 2004.

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